RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2814

PATENT APPLICATION
Docket No.: 8750-063
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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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| In re application of: | Hyoung-Sub KIM | | |
| Serial No.: | 10/771,749 | Examiner: | Cao, Phat X. |
| Filed: | February 3, 2004 | Group Art Unit: | 2814 |
| Confirmation No.: | 3653 | | |
| For: | SEMICONDUCTOR DEVICE HAVING SELF-ALIGNED CONTACT HOLE AND METHOD OF FABRICATING THE SAME | | |

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**RESPONSE AFTER FINAL REJECTION UNDER 37 CFR 1.116**

This paper is responsive to the Final Office Action (Paper No. 0206) that was mailed on 21 February 2006 and the Advisory Action (Paper No. 20060526) that was mailed on 31 May 2006.

**Claim Amendments** begin on page 2 of this paper.

**Remarks/Arguments** begin on page 5 of this paper.

## IN THE CLAIMS

1. (Currently amended) A semiconductor device comprising:

a semiconductor substrate having a cell array region and a peripheral circuit region;

a plurality of word line patterns placed on the cell array region, the word line patterns including a word line and a word line capping layer;

at least one gate pattern placed on the peripheral circuit region;

an interlayer insulating layer covering an upper surface of the semiconductor substrate having the word line patterns and the at least one gate pattern;

a self-aligned contact hole formed in the interlayer insulating layer between the word line patterns;

a self-aligned contact spacer covering a side wall of the self-aligned contact hole; ~~and~~

gate spacers interposed between side walls of the at least one gate pattern and the interlayer insulating layer, a width of the gate spacers being substantially different from a width of the self-aligned contact ~~spacer.~~ spacer;

word line spacers interposed between side walls of the word line patterns placed opposite to the self-aligned contact hole and the interlayer insulating layer, the word line spacers being formed of the same material layer as the gate spacer, a maximum width of the word line spacers substantially the same as a maximum width of the gate spacers; and

a spacer etch stop layer disposed in contact with the word line spacers and the word line patterns in the cell array region, disposed in contact with the gate spacers and the at least one gate pattern in the peripheral circuit region, and disposed in contact with the self-aligned contact spacer and the word line patterns in the cell array region.

2-3. (Cancelled)

4. (Currently amended) The semiconductor device according to ~~claim 2,~~ claim 1, further comprising:

a contact etch stop layer disposed in contact with the word line spacers and the interlayer insulating layer in the cell array region, and disposed in contact with the gate spacers and the interlayer insulating layer in the peripheral circuit region.

5. (Previously presented) The semiconductor device according to claim 1, wherein the interlayer insulating layer is one selected from the group consisting of an HDP oxide layer, a USG layer, and a PSG layer.

6. (Previously presented) The semiconductor device according to claim 1, the self-aligned contact hole comprising a lower contact hole and an upper contact hole, the lower contact hole formed at a region between the word line patterns and having a first diameter, the upper contact hole placed on the lower contact hole, disposed to penetrate the interlayer insulating layer, and having a second diameter that is unequal to the first diameter.

7. (Previously presented) The semiconductor device according to claim 6, the second diameter greater than the first diameter in a direction across the word line patterns.

8. (Original) The semiconductor device according to claim 1, wherein the width of the self-aligned contact spacer is smaller than the width of the gate spacers.

9. (Currently amended) A device comprising:

at least two word line patterns in a cell array region of a semiconductor substrate;

at least one gate pattern in a peripheral circuit region of the semiconductor substrate;

an inter-layer insulating layer covering the semiconductor substrate, the at least two word line patterns, and the at least one gate pattern, the at least one gate pattern including a gate spacer, the gate spacer disposed entirely between a sidewall of the at least one gate pattern and the inter-layer insulating layer;

a self-aligned contact hole penetrating the inter-layer insulating layer between the at least two word line patterns; ~~and~~

a self-aligned contact spacer on a sidewall of the self-aligned contact hole, a width of the self-aligned contact spacer unequal to a width of the gate ~~spacer.~~ spacer;

a word line spacer between one of the at least two word line patterns and the interlayer insulating layer, the word line spacer formed of the same material and having the same width as the gate spacer; and

a spacer etch stop layer disposed in contact with the word line spacer and one of the at least two word line patterns, disposed in contact with the gate spacer and the at least one gate pattern, and disposed in contact with the self-aligned contact spacer and the at least two word line patterns.

10-11. (Cancelled)

12. (Currently amended) The semiconductor device according to ~~claim 10~~, claim 9, further comprising:

a contact etch stop layer between the at least two word line spacers and the inter-layer insulating layer, and between the gate spacer and the inter-layer insulating layer.

13. (Original) The semiconductor device according to claim 9, the self-aligned contact hole comprising:

a lower contact hole; and

an upper contact hole, a diameter of the upper contact hole greater than a diameter of the lower contact hole in a direction perpendicular to the at least two word line patterns.

14-20. (Cancelled)

## REMARKS

Claims 2-3, 10-11 and 14-20 are cancelled. Claims 1, 4, 9 and 12 are amended. No new subject matter is added. Claims 1, 4-8, 9 and 12-13 remain pending in the application. Reconsideration and allowance of the pending claims is requested in light of the following remarks.

### *Allowable Subject Matter*

Claim 3 is objected to as being dependent upon a rejected base claim, but is otherwise indicated to be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

In keeping with this suggestion, claim 1 is amended to incorporate the subject matter of claims 2 and 3. Claims 2 and 3 are cancelled. Claim 4 is amended for consistency with claim 1. Therefore, claims 1 and 4-8 are placed in condition for allowance.

Further in keeping with this suggestion, claim 9 is amended to incorporate the subject matter of claims 10 and 11. Claim 9 is further amended to incorporate the subject matter of claim 3. Claims 10 and 11 are cancelled. Claim 12 is amended for consistency with claim 9. Therefore, claims 9 and 12-13 are placed in condition for allowance.

### *Claim Rejections – 35 U.S.C. § 102*

Claims 1-2, 4, 8-10 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,091,154 to Ohkawa ("Ohkawa"). The amendments to claims 1 and 9 render these rejections moot.

### *Claim Rejections – 35 U.S.C. § 103*

Claims 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohkawa in view of U.S. Patent No. 5,817,562 Chang, et al. ("Chang"). Claim 11 is cancelled, and the amendment of claim 1 renders the rejection of claim 5 moot.

Claims 6-7 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohkawa in view of U.S. Patent No. 6,649,503 Kim et al. ("Kim"). The amendments to claims 1 and 9 render these rejections moot.

***Conclusion***

For the reasons presented above, the pending claims are believed to be in condition for allowance, and such allowance is requested. Please telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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